PUSB3FS4

Extremely low capacitance unidirectional ESD protection diode array

13 December 2023 **Short data sheet**

1. General description

Extremely low capacitance unidirectional ElectroStatic Discharge (ESD) protection diode array, part of the TrEOS protection family. This device is housed in a DFN2510A-10 (SOT1176) leadless ultra small Surface-Mounted Device (SMD) plastic package, designed to protect four signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Unidirectional ESD protection for four signal lines
- V_{RWM} = 3.3 V device
- Extremely low clamping voltage to protect sensitive I/Os
- IEC 61000-4-5 (surge): I_{PP} = 8.2 A peak pulse (average measured)
- Extremely low diode capacitance C_d = 0.29 pF typical at 1.5 V
- ESD protection up to ±15 kV according to IEC 61000-4-2
- Leadless ultra small DFN2510A-10 (SOT1176) surface mount package

3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals
- USB3.2 and HDMI2.1 data lines

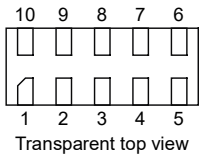
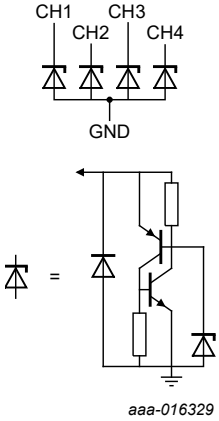
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage			-0.5	-	3.3	V
C_d	diode capacitance	f = 1 MHz; V_R = 1.5 V; pin 1; T_{amb} = 25 °C		-	0.29	0.34	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	 **DFN2510A-10 (SOT1176-2)**	
2	CH2	channel 2 ESD protection		
3	GND	ground		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	n.c.	not connected		
7	n.c.	not connected		
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3FS4	DFN2510A-10	plastic, extremely thin small outline package; no leads; 10 terminals; body 1.0 x 2.5 x 0.5 mm	SOT1176-2

7. Application information

The device is designed for the protection of four unidirectional data or signal lines from surge pulses and ESD damage.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

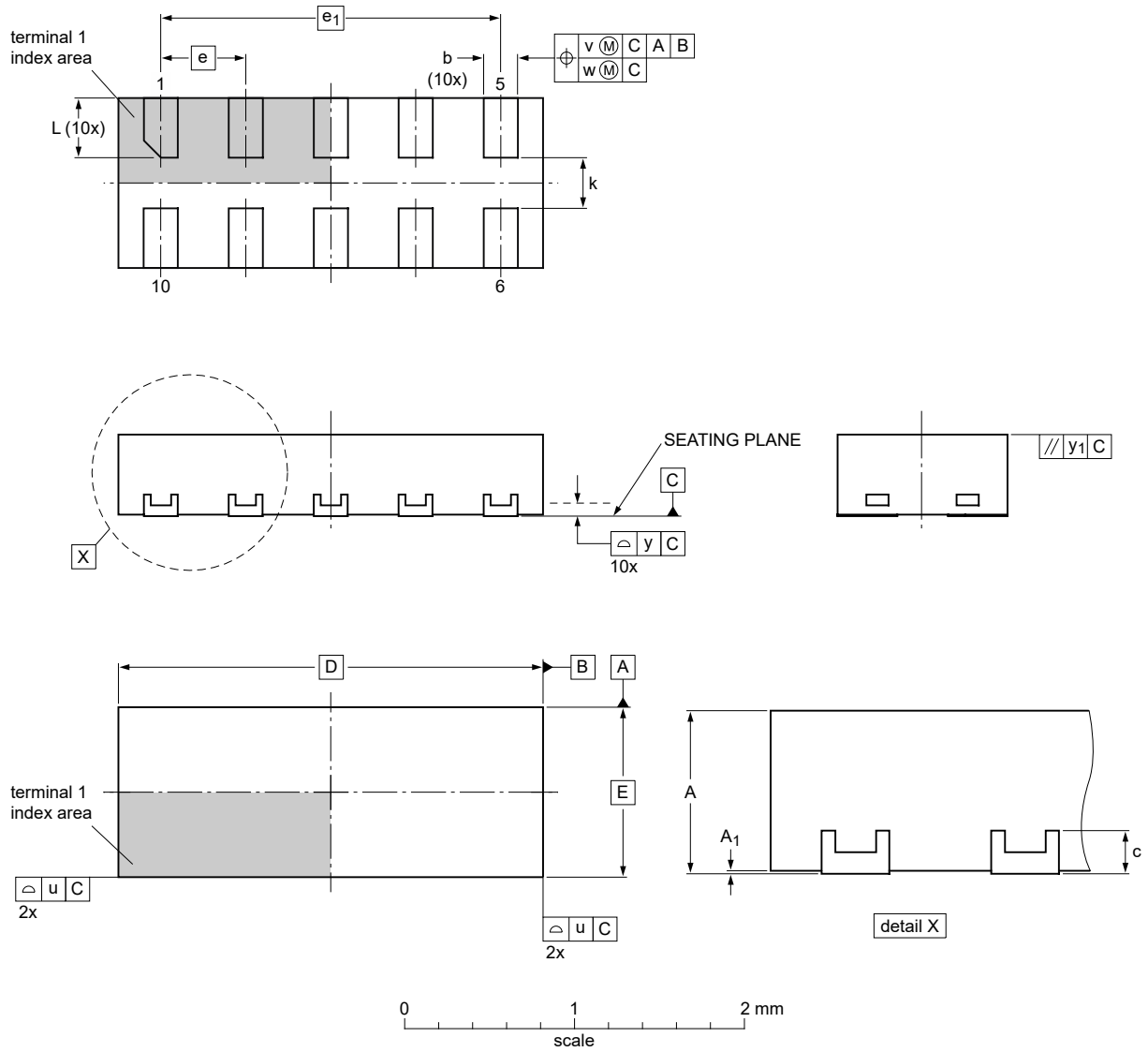
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

DFN2510A-10: plastic, extremely thin small outline package; no leads; 10 terminals; body 1.0 x 2.5 x 0.5 mm **SOT1176-2**



Dimensions

Unit[1]		A	A_1	b	c	D	E	e	e_1	k	L	u	v	w	y	y_1
mm	max	0.5	0.05	0.25	0.127 REF	2.5	1.0	0.5	2.0		0.40	0.1	0.1	0.05	0.05	0.05
	nom			0.20							0.35					
	min		0.00	0.15						0.2	0.30					

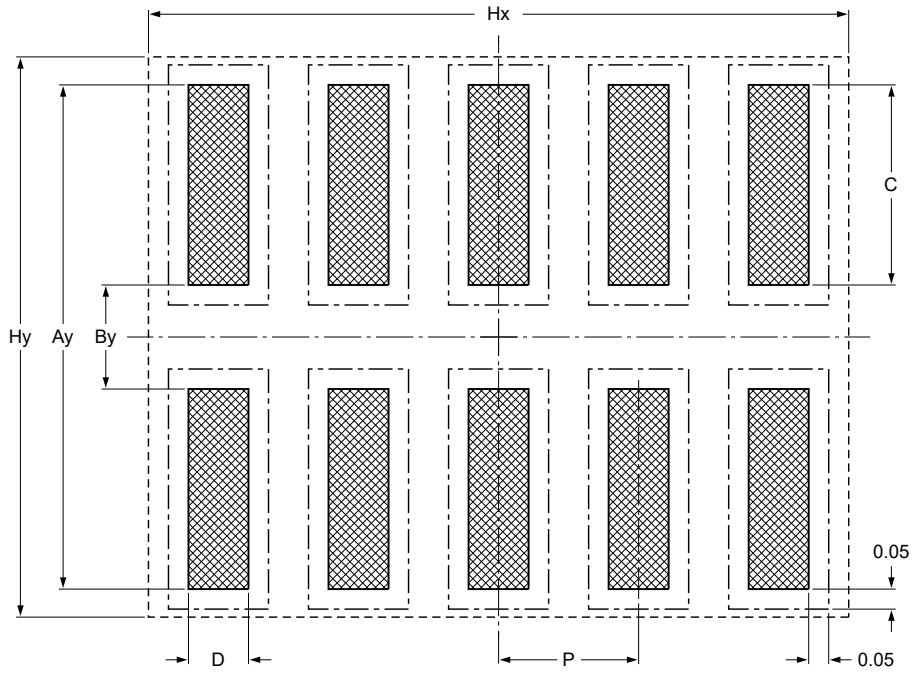
sot1176-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1176-2		---				~~21-07-05~~ 21-07-06

Fig. 1. Package outline DFN2510A-10 (SOT1176-2)

9. Soldering

Footprint information for reflow soldering of DFN2510A-10 package **SOT1176-2**



Generic footprint pattern
Refer to the package outline drawing for actual layout

recommended stencil thickness: 0.1 mm

occupied area
solder resist
solder paste
solder land

Dimensions in mm

P	Ay	By	C	D	Hx	Hy
0.5	1.25	0.3	0.475	0.2	2.45	1.5

Issue date 21-07-05

sot1176-2_fr

Fig. 2. Reflow soldering footprint for DFN2510A-10 (SOT1176-2)

10. Revision history

Table 4. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3FS4_SDS v.2	20231213	Short data sheet	-	PUSB3FS4_SDS v.1
Modifications:	• Package version corrected to SOT1176-2			
PUSB3FS4_SDS v.1	20230208	Short data sheet	-	-

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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