Micropower Hot Swap Controller

FEATURES

- **Enables Safe Board Insertion and Removal from a Power Supply**
- **4µA Supply Current**
- **0.3µA Shutdown Current**
- **Wide Operating Voltage Range: 2.7V to 36V**
- **Reverse Supply Protection to –40V**
- **Adjustable Analog Current Limit with Circuit Breaker**
- Automatic Retry or Latchoff on Current Fault
- Overvoltage and Undervoltage Monitoring
- Controls Single or Back-to-Back N-Channel MOSFETs
- 12-Lead MSOP and 3mm × 3mm QFN Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Battery Powered Equipment
- Solar Powered Systems
- Portable Instruments
- Automotive Battery Protection
- Energy Harvesting

DESCRIPTION

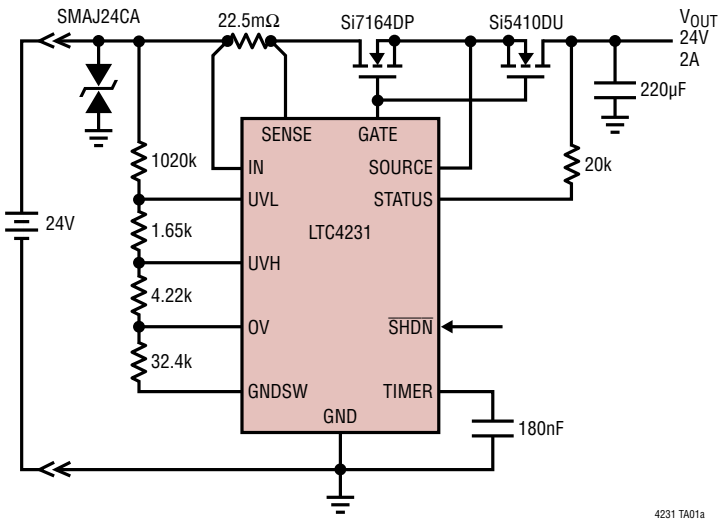
The LTC®4231 is a micropower Hot Swap controller that allows safe circuit board insertion and removal from a live power supply. An internal high side switch driver controls the gate of an external N-channel MOSFET. Back-to-back MOSFETs can be used for reverse supply protection down to –40V.

The LTC4231 provides a debounce delay and allows the GATE to be ramped up at an adjustable rate. After start-up, the LTC4231's quiescent current drops to 4µA during normal operation with output active. UVL, UVH, OV and GNDSW monitor overvoltage and undervoltage periodically, keeping total quiescent current low. Pulling $\overline{\text{SHDN}}$ low shuts down the LTC4231 and quiescent current drops to 0.3µA.

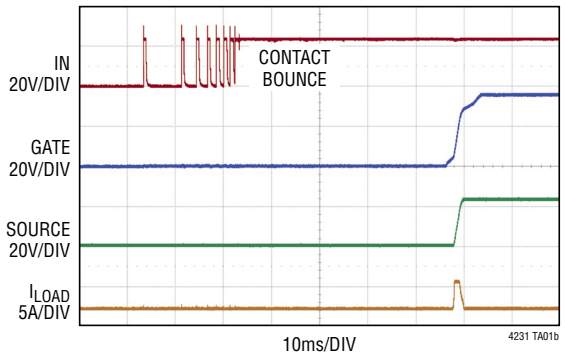
During an overcurrent fault, the LTC4231 actively limits current while running an adjustable timer. The LTC4231-1 remains off after a current fault while the LTC4231-2 automatically reapplies power after a cool-down period.

TYPICAL APPLICATION

Battery Hot Swap with Reverse Protection



Power-Up Waveforms



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage
- IN ..... –40V to 40V

Input Voltages
- SENSE, SOURCE ..... –40V to 40V
- IN–SENSE ..... –40V to 40V
- $\overline{SHDN}$, UVL, UVH, OV, GNDSW ..... –0.3V to 40V

Input Currents
- $\overline{SHDN}$, UVL, UVH, OV, GNDSW (Note 3) ..... –1mA

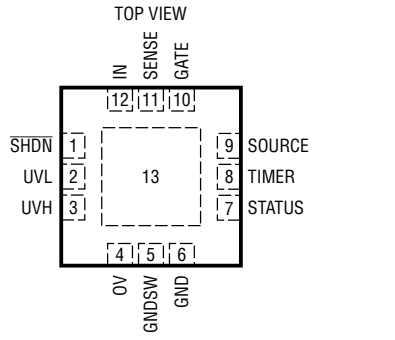
Output Voltages
- GATE–SOURCE (Note 4) ..... –0.3V to 13V
- GATE–SENSE ..... –40V to 20V
- STATUS ..... –0.3V to 40V
- TIMER ..... –0.3V to 4V

Operating Ambient Temperature Range
- LTC4231C ..... 0°C to 70°C
- LTC4231I ..... –40°C to 85°C
- LTC4231H ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

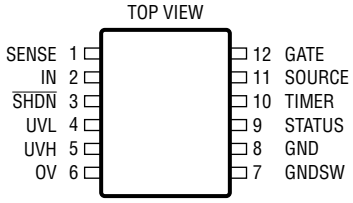
Lead Temperature (Soldering, 10 sec)
- MSOP Package ..... 300°C

PIN CONFIGURATION



UD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 68°C/W
EXPOSED PAD (PIN 13) PCB CONNECTION TO GND IS OPTIONAL



MS PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4231CUD-1#PBF	LTC4231CUD-1#TRPBF	LGMX	12-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC4231CUD-2#PBF	LTC4231CUD-2#TRPBF	LGSP	12-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC4231IUD-1#PBF	LTC4231IUD-1#TRPBF	LGMX	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC4231IUD-2#PBF	LTC4231IUD-2#TRPBF	LGSP	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC4231HUD-1#PBF	LTC4231HUD-1#TRPBF	LGMX	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC4231HUD-2#PBF	LTC4231HUD-2#TRPBF	LGSP	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC4231CMS-1#PBF	LTC4231CMS-1#TRPBF	42311	12-Lead Plastic MSOP	0°C to 70°C
LTC4231CMS-2#PBF	LTC4231CMS-2#TRPBF	42312	12-Lead Plastic MSOP	0°C to 70°C
LTC4231IMS-1#PBF	LTC4231IMS-1#TRPBF	42311	12-Lead Plastic MSOP	–40°C to 85°C
LTC4231IMS-2#PBF	LTC4231IMS-2#TRPBF	42312	12-Lead Plastic MSOP	–40°C to 85°C
LTC4231HMS-1#PBF	LTC4231HMS-1#TRPBF	42311	12-Lead Plastic MSOP	–40°C to 125°C
LTC4231HMS-2#PBF	LTC4231HMS-2#TRPBF	42312	12-Lead Plastic MSOP	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS**				
LTC4231IMS-1#WPBF	LTC4231IMS-1#WTRPBF	42311	12-Lead Plastic MSOP	–40°C to 85°C
LTC4231IMS-2#WPBF	LTC4231IMS-2#WTRPBF	42312	12-Lead Plastic MSOP	–40°C to 85°C
LTC4231HMS-1#WPBF	LTC4231HMS-1#WTRPBF	42311	12-Lead Plastic MSOP	–40°C to 125°C
LTC4231HMS-2#WPBF	LTC4231HMS-2#WTRPBF	42312	12-Lead Plastic MSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. IN = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN							
V_{IN}	Input Supply Voltage Range		●	2.7		36	V
$V_{IN(UVL)}$	Input Supply Undervoltage Lockout	IN Rising	●	2	2.3	2.6	V
$\Delta V_{IN(HYST)}$	Input Supply Undervoltage Lockout Hysteresis				200		mV
I_{CC}	Supply Current (Average)	(Note 5)					
	Normal On, Voltage or Current Fault	$I_{GATE} \leq -0.1\mu A$, $C_{GATE-SOURCE}$ = 1nF, (C-Grade, I-Grade)	●		4	10	µA
		(H-Grade)	●		4	20	µA
	Start-Up or Overcurrent		●		300	600	µA
	Shutdown	$\overline{SHDN}$ Low, GATE Pulled to GND, (C-Grade, I-Grade)	●		0.3	1	µA
		(H-Grade)	●		0.3	2	µA
	Reverse Input	IN, SENSE = –40V	●		–2.5	–5	mA
SENSE							
$\Delta V_{SENSE(CB)}$	Circuit Breaker Threshold ($V_{IN} - V_{SENSE}$)		●	47	50	53	mV
$\Delta V_{SENSE(ACL)}$	Analog Current Limit	During Output Short-Circuit	●	65	80	90	mV
I_{SENSE}	SENSE Input Current	$\overline{SHDN}$ = High, SENSE = 12V	●		0.3	1	µA
GATE, SOURCE							
ΔV_{GATE}	External N-Channel Gate Drive ($V_{GATE} - V_{SOURCE}$)	V_{IN} < 7V, I_{GATE} = 0, –0.1µA	●	4.5	6.2	10	V
		$V_{IN} \geq$ 7V, I_{GATE} = 0, –0.1µA	●	10	11.4	18	V
$\Delta V_{GATE(H)}$	ΔV_{GATE} ($V_{GATE} - V_{SOURCE}$) Threshold That Deactivates the Charge Pump	V_{IN} < 7V	●	5.5	6.5	10	V
		$V_{IN} \geq$ 7V	●	11	11.7	18	V
$V_{GATE(L)}$	GATE Low Threshold	To Enter Shutdown or Voltage Fault	●	0.4	1.2	1.8	V
$I_{GATE(UP)}$	GATE Pull-Up Current	GATE On, GATE = 1V	●	–7	–10	–13	µA
$I_{GATE(FAST)}$	GATE Fast Pull-Down Current	ΔV_{SENSE} = 0.5V, ΔV_{GATE} = 5V	●	70	130		mA
$I_{GATE(SLOW)}$	GATE Slow Pull-Down Current	$\overline{SHDN}$ = 0V, ΔV_{GATE} = 5V	●	0.6	1		mA
$t_{D(ON)}$	Turn-On Debounce Delay	UVL = UVH = 2V, OV = 0V, $\overline{SHDN}$ = Step 0V to 5V	●	20	40	60	ms
t_{RETRY}	Auto-Retry Delay	LTC4231-2	●	0.27	0.5	0.73	s
$t_{PHL(ILIM)}$	Overcurrent to GATE Low Propagation Delay	ΔV_{SENSE} = Step 0mV to 300mV, C_{GATE} = 1nF, ΔV_{GATE} Crosses 1V	●		0.5	1	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. IN = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
UVL, UVH, OV, GNDSW, STATUS and $\overline{SHDN}$							
V_{UV}	UVL, UVH Threshold		●	0.776	0.795	0.814	V
V_{OV}	OV Threshold	OV Rising	●	0.776	0.795	0.814	V
$V_{OV(HYST)}$	OV Hysteresis		●	3	15	30	mV
$I_{LEAK(0.9V)}$	UVL, UVH and OV Leakage Current	V = 0.9V (C-Grade, I-Grade) (H-Grade)	● ●		0 0	±10 ±100	nA nA
$I_{LEAK(12V)}$	UVL, UVH, OV, GNDSW, STATUS and $\overline{SHDN}$ Leakage Current	V = 12V (C-Grade, I-Grade) (H-Grade)	● ●		0 0	±100 ±500	nA nA
$R_{ON(GNDSW)}$	Switch Resistance		●		80	200	Ω
V_{OL}	STATUS Output Low Voltage	I = 2mA	●		0.2	0.4	V
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Threshold		●	0.4	0.8	1.5	V
t_{PERIOD}	Sampling Period		●	5	10	15	ms
t_{SAMPLE}	Sampling Width		●	100	200	300	µs
TIMER							
t_{CB}	Circuit Breaker Delay	C_T = 100nF	●	1.7	2.4	3.5	ms
$V_{TIMER(H)}$	TIMER High Threshold	TIMER Rising	●	1.170	1.193	1.216	V
$V_{TIMER(L)}$	TIMER Low Threshold	TIMER Falling	●	0.07	0.1	0.13	V
$I_{TIMER(UP)}$	TIMER Pull-Up Current	TIMER = 0.5V, Circuit Breaker Tripped	●	–35	–50	–65	µA
$I_{TIMER(DN)}$	TIMER Pull-Down Current	TIMER = 0.5V, Circuit Breaker Recovery	●	3	5	7	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

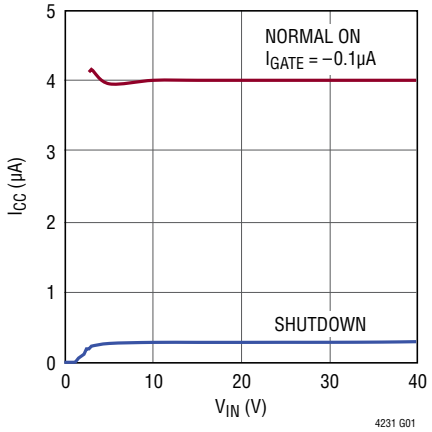
Note 3: These pins can be tied to voltages below –0.3V through a resistance that limits the current below 1mA.

Note 4: An internal clamp limits GATE to a minimum of 13V above SOURCE. Driving this pin to voltages beyond this clamp may damage the device.

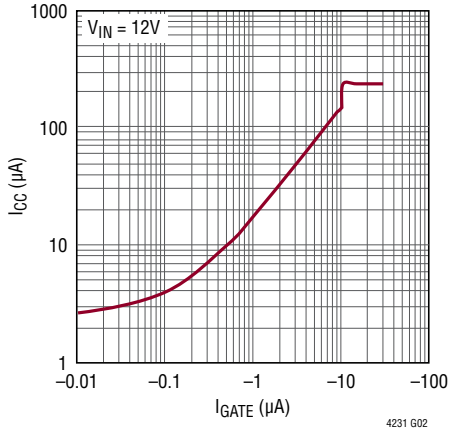
Note 5: For modes where GATE is pulled to GND, $I_{CC} = I_{IN} + I_{SENSE}$. Else $I_{CC} = I_{IN} + I_{SENSE} + I_{SOURCE}$.

TYPICAL PERFORMANCE CHARACTERISTICS

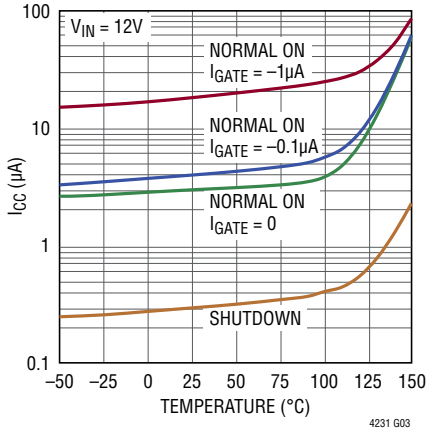
Average Supply Current vs IN



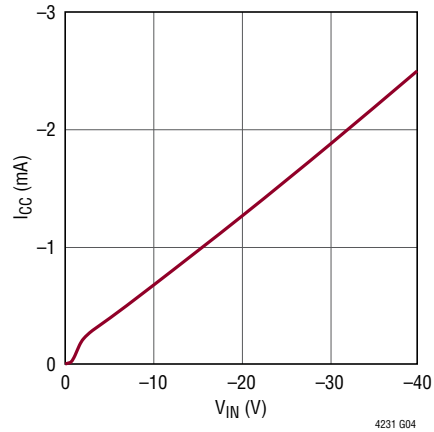
Average Supply Current (Normal On) vs GATE Leakage



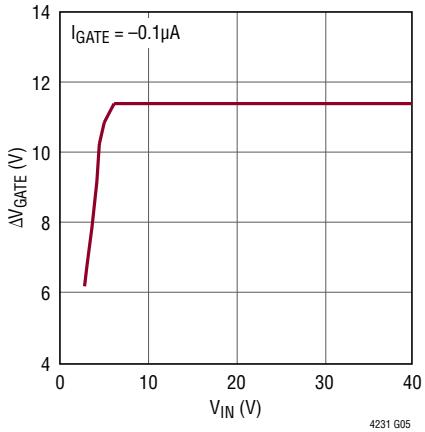
Average Supply Current vs Temperature



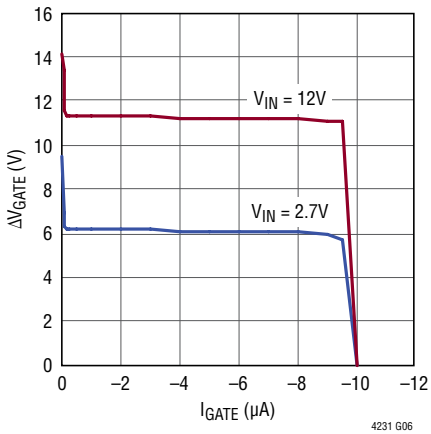
Supply Current (Reverse Input) vs IN



ΔV_{GATE} (Average) vs IN

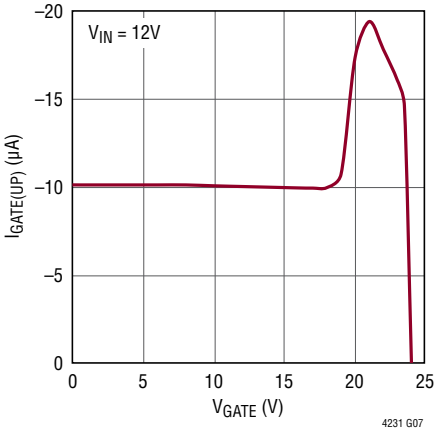


ΔV_{GATE} (Average) vs GATE Leakage

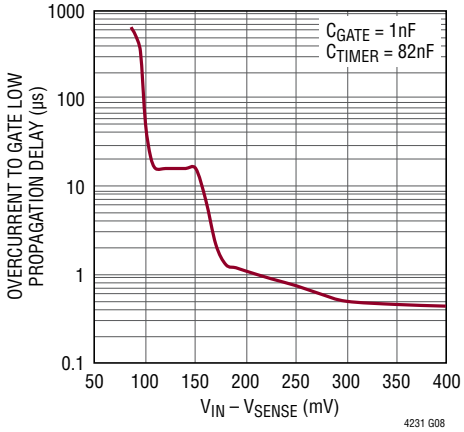


TYPICAL PERFORMANCE CHARACTERISTICS

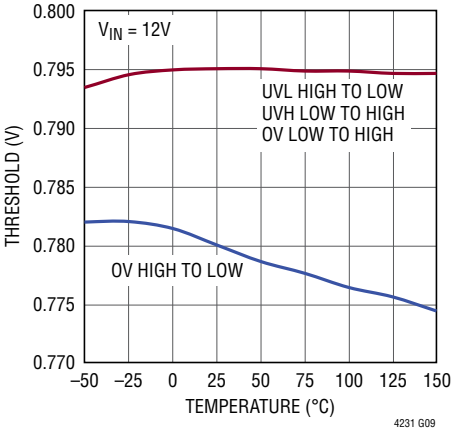
GATE Pull-Up Current vs V_{GATE}



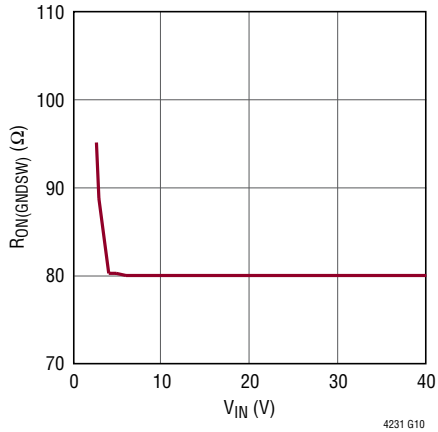
Overcurrent to GATE Low Propagation Delay



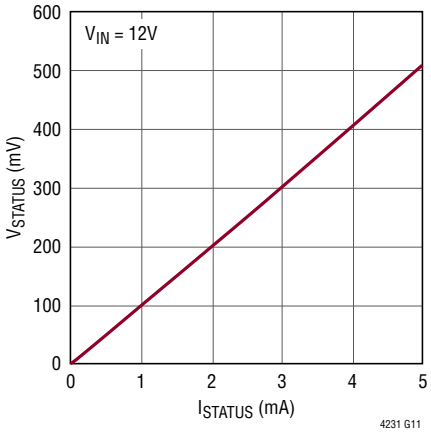
UVL, UVH, OV Thresholds vs Temperature



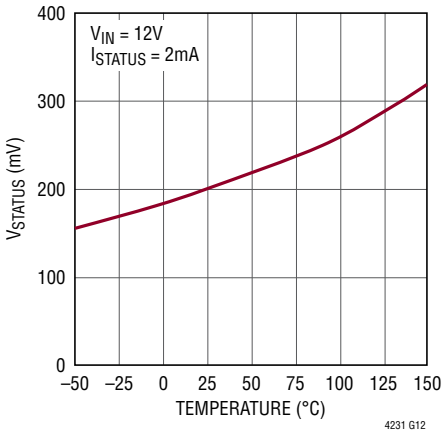
GNDSW Switch Resistance vs IN



STATUS Output Low Voltage vs Current



STATUS Output Low Voltage vs Temperature



PIN FUNCTIONS

GATE: Gate Drive for External N-Channel MOSFET. After all start-up conditions are satisfied, a 10µA pull-up current from the internal charge pump charges up ΔV_{GATE} to the high threshold voltage $\Delta V_{GATE(H)}$ and then turns off. The charge pump turns on again when ΔV_{GATE} decays by more than 0.7V or every 15ms, whichever comes first, and recharges ΔV_{GATE} to $\Delta V_{GATE(H)}$. During GATE turn-off, a 1mA pull-down current discharges GATE to GND. During severe short circuits, a 130mA pull-down current is activated to discharge GATE to SOURCE.

GND: Device Ground.

GNDSW: Switched GND. Connect this pin to an external resistive network to monitor IN for overvoltage or undervoltage (OV/UV). To reduce the power dissipated by this resistive divider, the LTC4231 periodically samples IN by connecting GNDSW to GND once every 10ms. Tie this pin to GND if unused.

IN: Supply Voltage and Current Sense Input. This pin has a nominal undervoltage lockout threshold of 2.3V.

$\overline{\text{SHDN}}$: Shutdown Control Input. A logic high at $\overline{\text{SHDN}}$ enables the LTC4231. GATE ramps up after a debounce delay of 40ms. A logic low at $\overline{\text{SHDN}}$ activates a 1mA pull-down current at GATE, discharging it to GND. Once GATE < 1.2V, the LTC4231 enters a low current Shutdown. Connect to IN if unused. When connected to IN, if IN goes below ground, use a resistor to limit the current to ≤1mA.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive network to monitor IN for OV. This pin connects internally to an overvoltage comparator with a 0.795V threshold. To reduce the power dissipated by this resistive divider, the LTC4231 periodically samples IN by connecting GNDSW to GND once every 10ms. Once an OV is detected at IN, GATE and STATUS pull low. Tie this pin to GND if unused.

SENSE: Current Sense Input. Connect to the output of the current sense resistor. The circuit breaker comparator and the analog current limit amplifier monitor the voltage across the current sense resistor. During an overcurrent fault when ΔV_{SENSE} exceeds 50mV, the circuit breaker comparator trips and triggers TIMER to ramp up. For more severe overcurrent faults, the analog current limit amplifier controls the gate of the external MOSFET to keep ΔV_{SENSE} at 80mV. To disable the circuit breaker comparator and analog current limit amplifier, connect this pin to IN.

SOURCE: N-Channel MOSFET Source Connection. Connect this pin to the source of the external MOSFET.

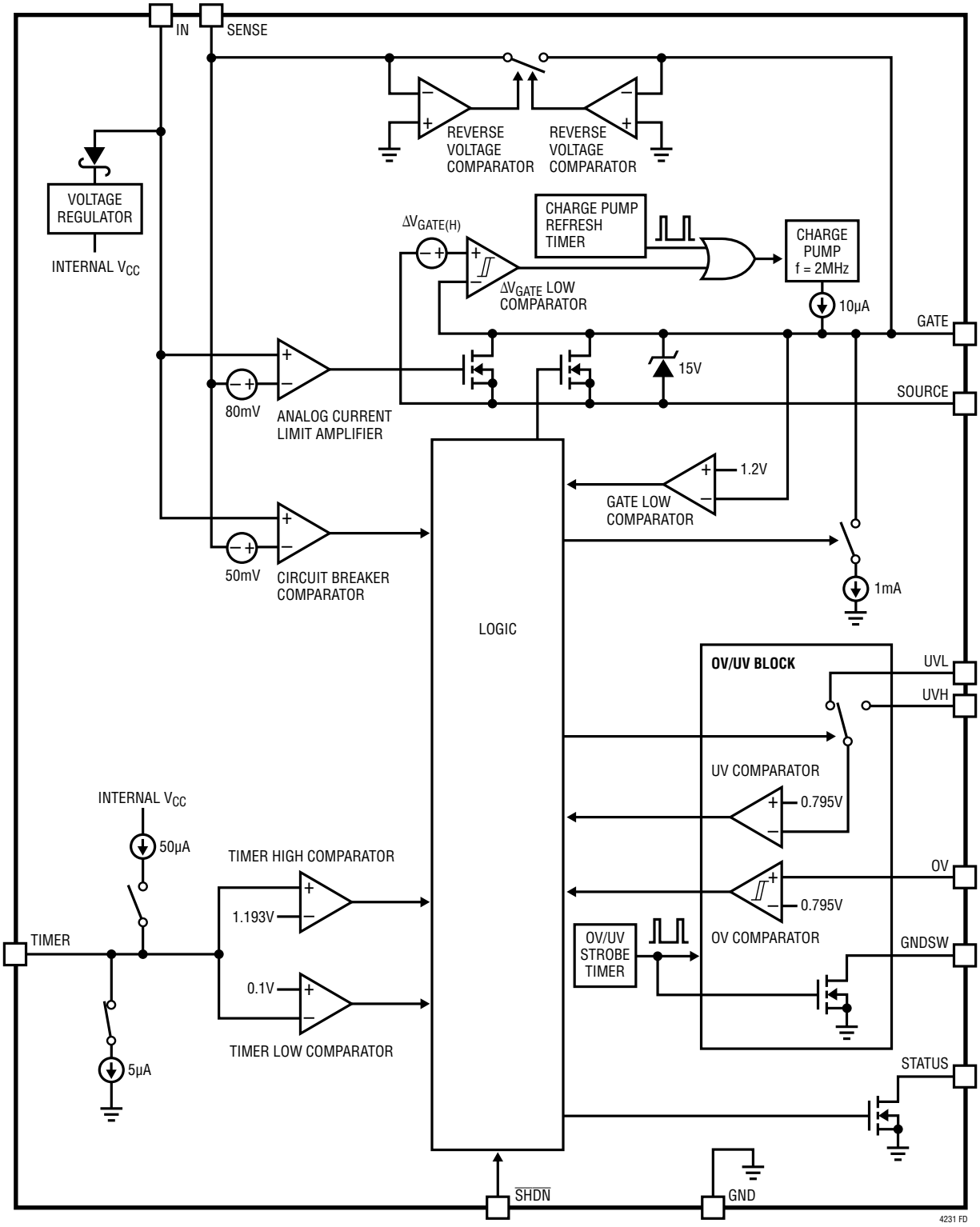
STATUS: Status Output. Open-drain output that goes high impedance when ΔV_{GATE} first exceeds $\Delta V_{GATE(H)}$. The state of the pin is latched and resets (pulls low) when $\overline{\text{SHDN}}$ goes low, an UVLO occurs, an OV/UV is detected at IN or an overcurrent fault sets the internal current fault latch. This pin may be left open if unused.

TIMER: Timer Input. Connect a capacitor between this pin and GND to set a 24ms/µF duration for overcurrent before the internal current fault latch trips and turns off the MOSFET. For the LTC4231-1 latchoff option, the MOSFET remains off until the current fault latch is cleared by pulling $\overline{\text{SHDN}}$ low or by cycling power. For the LTC4231-2 auto-retry option, the current fault latch is cleared automatically and the GATE is ramped up after a 500ms delay.

UVH, UVL: Undervoltage Comparator Input. Connect these pins to an external resistive network to monitor IN for UV. These pins connect internally to an undervoltage comparator with a 0.795V threshold. The comparator monitors UVH when GATE is low and UVL when GATE is high to implement separate undervoltage turn-on and undervoltage turn-off thresholds. To reduce the power dissipated by this resistive divider, the LTC4231 periodically samples IN by connecting GNDSW to GND once every 10ms. Once an UV is detected at these pins, GATE and STATUS pull low. Tie both pins to IN if unused. When connected to IN, for applications where IN goes below ground, use a resistor to limit the current to ≤1mA.

Exposed Pad (QFN Package): The exposed pad may be left open or connected to device ground.

FUNCTIONAL DIAGRAM



OPERATION

The LTC4231 is a micropower Hot Swap controller that controls an external N-channel MOSFET to turn on and off a supply voltage in a controlled manner. This allows a circuit to be safely inserted and removed from a powered connector without glitches or connector damage from uncontrolled inrush current.

When the LTC4231 is first powered up, the gate of the MOSFET is held at GND to keep it off. Pulling $\overline{SHDN}$ high and IN above undervoltage lockout (UVLO) starts an internal clock that monitors the resistive divider at IN once every 10ms by connecting GNDSW to GND. A 40ms debounce cycle is also started. Average I_{CC} during this debounce mode is 4µA.

After the 40ms debounce cycle, the LTC4231 goes into start-up mode to ramp up GATE. In this mode, all circuits blocks except the overvoltage or undervoltage (OV/UV) block are activated and I_{CC} = 300µA. The internal charge pump supplies a 10µA pull-up current to GATE. Once ΔV_{GATE} exceeds $\Delta V_{GATE(H)}$, STATUS goes high impedance. This indicates that GATE is high and the power path is on. Average I_{CC} drops to 4µA during this normal on mode as some circuit blocks are shut down and the internal charge pump periodically turns on to recharge GATE as needed. The periodic monitoring of the IN resistive divider continues as long as $\overline{SHDN}$ is high and IN ≥ 2.3V.

If an OV/UV violation is detected during the IN monitoring time, the part goes into voltage fault mode (average I_{CC} = 4µA) where GATE and STATUS is pulled to GND. The debounce cycle restarts when no OV/UV violation is detected during a subsequent IN monitoring window.

The LTC4231 has a circuit breaker comparator that monitors the voltage across the current sense resistor. This comparator trips when ΔV_{SENSE} exceeds 50mV, bringing the LTC4231 into overcurrent mode. In this mode, all circuits blocks except the OV/UV block are activated and I_{CC} = 300µA. If ΔV_{SENSE} > 80mV, the analog current limit amplifier limits ΔV_{SENSE} to 80mV by servoing ΔV_{GATE} in an active control loop. The TIMER capacitor is ramped up with a 50µA pull-up when ΔV_{SENSE} > 50mV. When TIMER > 1.193V, the current fault latch is set, causing GATE and STATUS to pull low. The part goes into current fault mode.

In current fault mode, the latchoff (LTC4231-1) version keeps TIMER and GATE low. The auto-retry (LTC4231-2) version waits 500ms before GATE is ramped up again. For both versions, the part can be reset by cycling $\overline{SHDN}$ low then high or by cycling IN to GND and back. After the reset, the LTC4231 goes through a debounce cycle before re-starting GATE.

$\overline{SHDN}$ acts as a shutdown switch for the supply path. When it goes high, the LTC4231 ramps GATE up after a debounce cycle to turn on the external MOSFET. When it goes low, GATE is pulled to GND to turn off the external MOSFET. The LTC4231 then goes into shutdown mode where I_{CC} drops to 0.3µA.

IN, SENSE, GATE and SOURCE are protected against reverse inputs of up to –40V. Two reverse voltage comparators detect negative input potentials at SENSE or GATE and quickly connect GATE to SENSE. When used with back-to-back MOSFETs as shown in Figure 5, this feature will isolate the load from a negative input.

APPLICATIONS INFORMATION

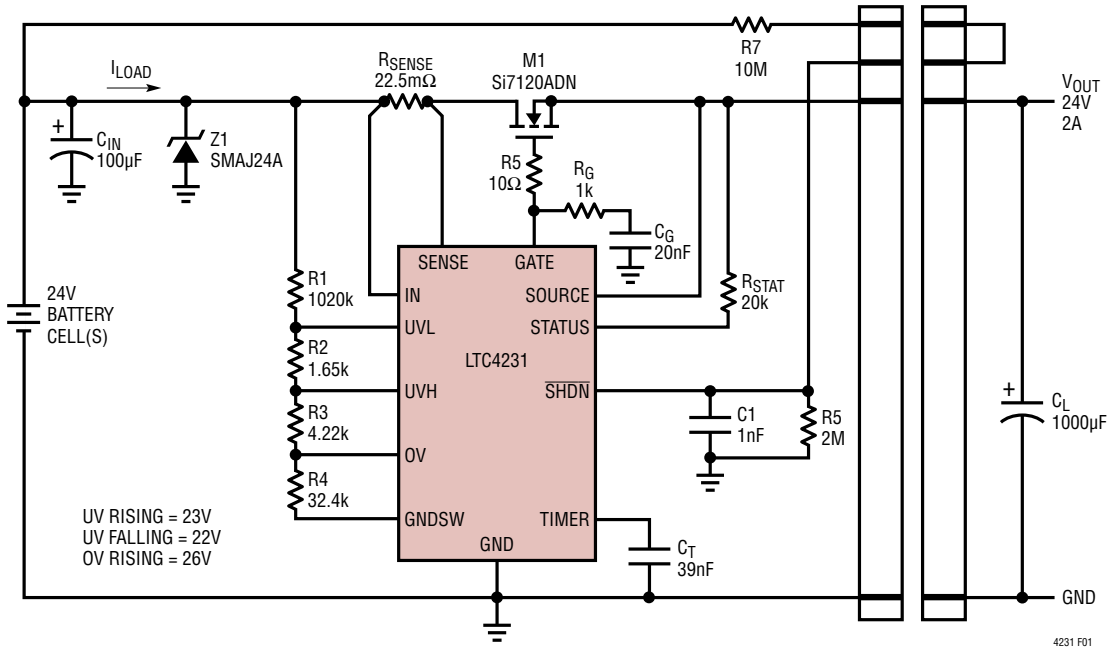


Figure 1. Channel Controller with Connector Enable

The micropower capability of the LTC4231 makes it ideal for Hot Swap applications in battery powered systems where current load is light or intermittent and power draw is a concern. It can implement battery short circuit protection, reverse battery protection, battery voltage monitoring, power path control, hot-plug and inrush current control in off-grid, autonomous systems.

Turn-On Sequence

When IN is less than the UVLO level of 2.3V or $\overline{SHDN}$ is low, GATE is pulled to GND and STATUS pulls low. When IN ≥ 2.3V and $\overline{SHDN}$ goes high, an internal clock starts timing a 40ms debounce cycle. The clock also times a 200µs strobe of the resistive divider at IN every 10ms to make sure IN is not in OV/UV. Average I_{CC} during this debounce mode is 4µA.

Any OV/UV detected will stop and reset the debounce timing cycle. During this voltage fault mode, average I_{CC} is 4µA. The debounce cycle only restarts when a subsequent IN strobe indicates that the input power is within the acceptable range, IN ≥ 2.3V and $\overline{SHDN}$ is high.

When the debounce cycle of 40ms successfully completes, the LTC4231 turns on its charge pump, analog current limit amplifier and TIMER control circuit blocks as it goes into start-up mode (I_{CC} = 300µA). The external MOSFET is turned on by charging up the GATE with a 10µA charge pump generated current source.

At start-up, the MOSFET current is typically dominated by the current charging the load capacitor C_L. If ΔV_{SENSE} > 80mV, the analog current limit amplifier controls the gate of the MOSFET in a closed loop. This keeps the start-up inrush current at 80mV/R_{SENSE}. When ΔV_{SENSE} > 50mV, the TIMER capacitor charges up with an internal 50µA pull-up current.

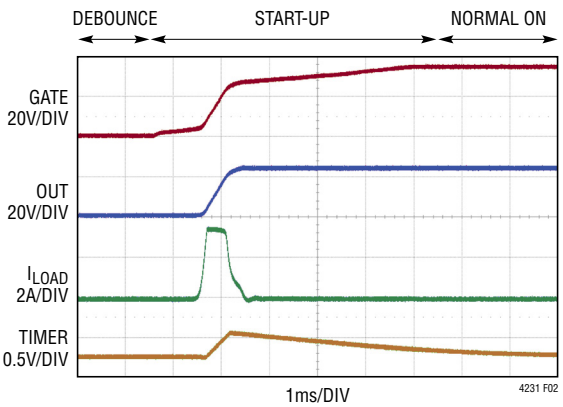


Figure 2. Inrush Control by Analog Current Limit

APPLICATIONS INFORMATION

In most applications, keeping the inrush current at analog current limit is an acceptable start-up method if the TIMER delay is long enough to avoid setting the current fault latch and the MOSFET has adequate safe operating margin. However, for more flexibility in design (See the Design Example section), a capacitor from GATE to GND (Figure 1) can be used to limit the V_{GATE} slew rate for inrush current control. V_{GATE} rises with a slope equal to $10\mu A/C_G$ (Figure 3). The supply inrush current is then limited to:

$$I_{INRUSH} = \frac{C_L}{C_G} \bullet 10\mu A$$

Once ΔV_{GATE} exceeds $\Delta V_{GATE(H)}$, STATUS goes high impedance. I_{CC} drops from 300µA to 4µA (average) during this normal on mode as some circuit blocks are shut down and the internal charge pump periodically turns on when ΔV_{GATE} droops by 0.7V or every 15ms, whichever comes first (Figure 7).

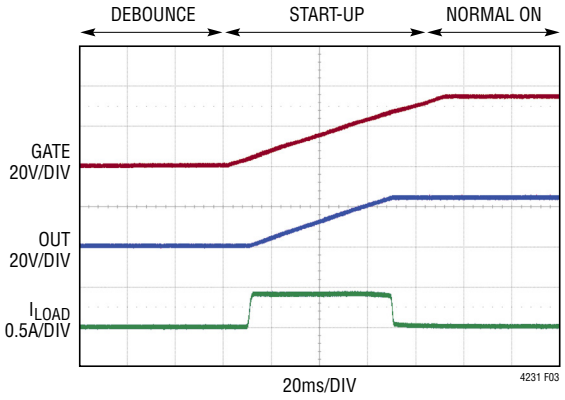


Figure 3. Inrush Control by Limiting V_{GATE} Slew

Turn-Off Sequence

The MOSFET switch can be turned off by $\overline{SHDN}$ going low, an OV/UV event, an overcurrent setting the current fault latch or IN dropping below its UVLO voltage. Under any of these conditions, STATUS pulls low and the MOSFET is turned off with a 1mA current pulling down from GATE to GND.

In the back-to-back MOSFET configuration as shown in Figure 5, SOURCE will also be pulled to GND via the parasitic body diode between GATE and SOURCE, cutting off the load from IN. This configuration is suitable in power path control and reverse battery protection applications where IN is likely to go below GND.

In the single MOSFET configuration (Figure 1), the 1mA pull-down from GATE to GND also discharges the load capacitor C_L to GND once GATE goes below SOURCE.

Overcurrent Fault

The 50mV circuit breaker threshold sets the maximum load current allowed under steady state conditions. However, the LTC4231 allows mild overcurrents during supply or load transients when ΔV_{SENSE} momentarily exceeds 50mV but stays below the 80mV analog current limit threshold. For severe overcurrents when ΔV_{SENSE} exceeds 80mV, the analog current limit amplifier controls ΔV_{GATE} to regulate ΔV_{SENSE} to 80mV. The durations of these transient overcurrents must be less than the circuit breaker delay (t_{CB}) which can be adjusted using the capacitor C_T at the TIMER pin.

When ΔV_{SENSE} exceeds 50mV, the LTC4231 goes into overcurrent mode. C_T is charged with a 50µA pull-up. If the overcurrent is transient and ΔV_{SENSE} goes below 50mV before TIMER reaches 1.193V, the 50µA pull-up on TIMER switches to a 5µA pull-down. Multiple overcurrents with a duty cycle > 10% can thus eventually integrate TIMER to 1.193V. When TIMER reaches 1.193V, the LTC4231 goes into current fault mode and sets an internal current fault latch. The external MOSFET will be cut off by a 1mA pull-down from GATE to GND while STATUS pull-down is asserted.

The time in which LTC4231 stays in overcurrent mode before going into current fault mode is called the circuit breaker delay and is given by:

$$t_{CB} = C_T \bullet 24\ [ms/\mu F]$$

APPLICATIONS INFORMATION

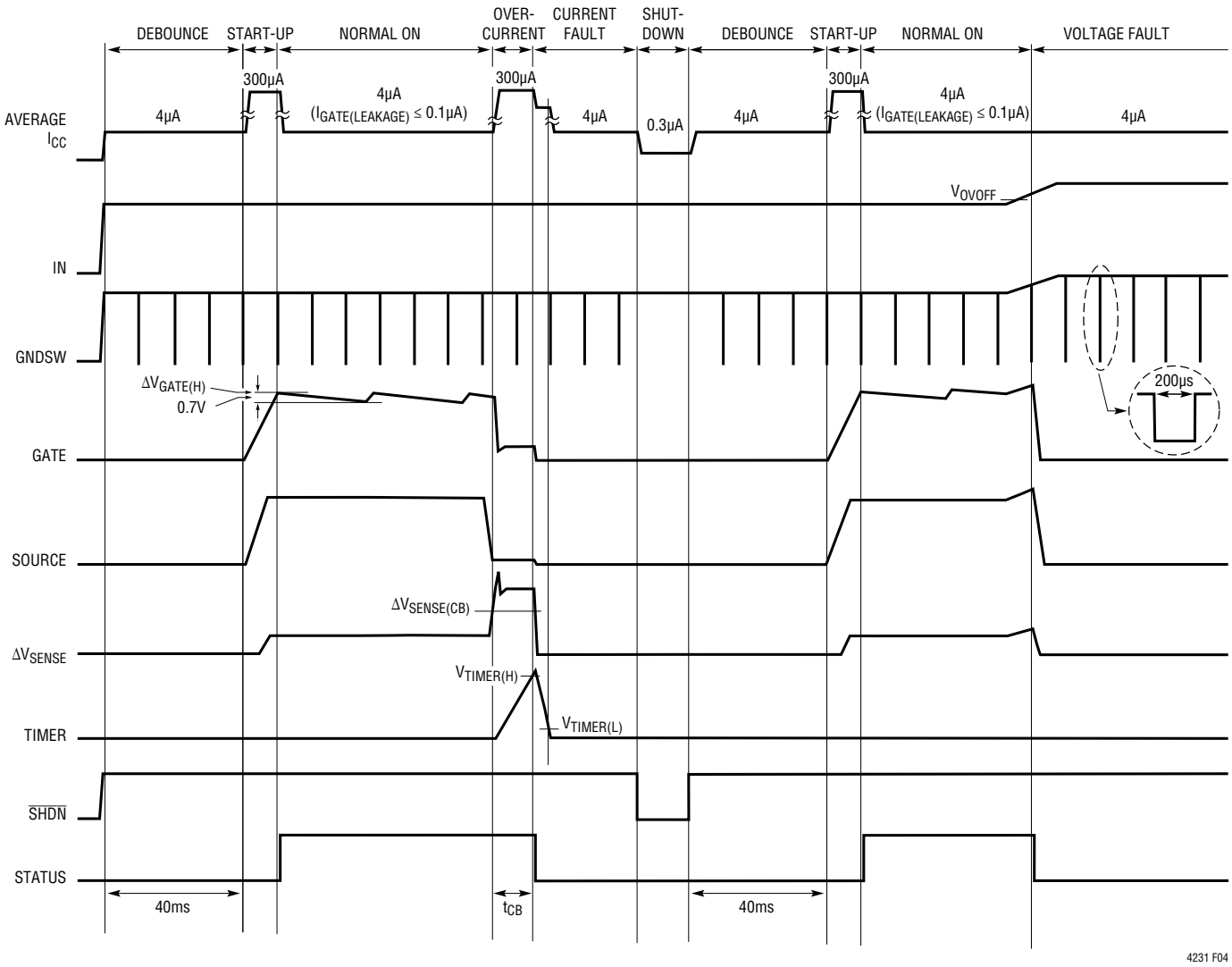


Figure 4. LTC4231-1 Overcurrent

APPLICATIONS INFORMATION

Auto-Retry vs Latchoff

During current fault mode, GATE is held low and TIMER is discharged to GND. Once TIMER < 0.1V, average I_{CC} goes to 4µA and the internal current fault latch is ready to be reset. The LTC4231-2 (automatic retry) waits for a 500ms retry delay after which the internal current fault latch is reset and GATE ramps up to turn the MOSFET back on.

The LTC4231-1 (latchoff) version does not restart automatically. Pulling $\overline{SHDN}$ low for >100µs will reset the internal current fault latch. When $\overline{SHDN}$ goes high, GATE ramps up after a debounce cycle. Alternatively, IN can be pulled to GND for >100µs then cycled back up again. This UVLO event will reset the internal current fault latch and GATE ramps up after a debounce cycle. A UV/OV detected at IN also resets the internal current fault latch and GATE ramps up after a debounce delay.

Analog Current Limit Loop Stability

The analog current limit loop on GATE is compensated by the parasitic gate capacitance of the external MOSFET. No further compensation components are normally required. If a small MOSFET with $C_{ISS} \leq 1nF$ is chosen, an R_G and C_G compensation network connected at GATE may be required (Figure 1) to ensure stability. The resistor, R_G, connected in series with C_G accelerates the MOSFET gate recovery after a fast gate pull-down. The value of C_G should be ≤100nF. An additional 10Ω resistor (R5 in Figure 1) should be added close to the MOSFET gate to prevent possible parasitic oscillation due to trace/wire inductance and capacitance.

Monitor OV and UV Faults

When IN is above UVLO and $\overline{SHDN}$ is high, an internal clock times a 200µs strobe of the resistive divider at IN every 10ms. During this 200µs strobe, the normally high impedance GNDSW is connected to GND with an internal 80Ω switch and the comparators connected to UVH, UVL and OV are awakened from sleep mode. The comparators sense the voltages on the resistive divider, and their outputs are latched at the end of the strobe window.

If an OV or UV violation is detected, the STATUS pulls low and a 1mA pull-down will be activated between GATE and GND to turn off the external MOSFET. When GATE goes <1.2V, average I_{CC} drops to 4µA as the LTC4231 goes into voltage fault mode. It stays in this mode until a subsequent IN strobe sees no OV/UV. The LTC4231 then re-starts after a debounce cycle.

Strobing the resistive divider reduces power consumption as the external resistors as well as the internal OV/UV comparators do not dissipate power in between strobes. For a 1M string of resistors used to monitor a V_{IN} of 24V, this strobing scheme reduces the current consumption from 24µA to 0.48µA as the strobing duty cycle is 2% (200µs/10ms). The OV/UV comparators dissipate 35µA during IN strobing. The 2% duty cycle reduces this to an average current of 0.7µA. Note that the response time to an OV/UV event can be as long as 10ms.

The four resistors allow three thresholds to be configured. They are the UV rising threshold (V_{UVON}), the UV falling threshold (V_{UVOFF}) and the OV rising threshold (V_{OVOFF}). The OV falling threshold is set by internal hysteresis to be 1.8% below the OV rising threshold. Using the comparator threshold as 0.795V and choosing appropriate values for R_{TOTAL} and R4, the resistor values can be calculated as follows:

$$R_{TOTAL} = R1 + R2 + R3 + R4$$

$$R4 = \left(\frac{0.795V}{V_{OVOFF}}\right) \bullet R_{TOTAL}$$

$$R3 = \left(\frac{V_{OVOFF}}{V_{UVON}} - 1\right) \bullet R4$$

$$R2 = \left(\frac{V_{UVON}}{V_{UVOFF}} - 1\right) \bullet \left(\frac{V_{OVOFF}}{V_{UVON}}\right) \bullet R4$$

$$R1 = \left(\frac{U_{OVOFF}}{0.795V} - 1\right) \bullet R4 - R3 - R2$$

It is recommended that the total value of the resistor string be less than 2M and traces at UVH, UVL, and OV kept short to minimize parasitic capacitance and improve settling time.

APPLICATIONS INFORMATION

Reverse Input Protection

Negative voltages at IN can occur if a battery is plugged in backwards or a negative supply is inadvertently connected. Back-to-back N-channel MOSFETs can be used as in Figure 5 to prevent the negative voltage from passing to the output load.

IN, SENSE, GATE and SOURCE are protected against reverse inputs of up to –40V. When the LTC4231's reverse voltage comparators detect a negative voltage at SENSE, an internal switch is activated to connect GATE to SENSE. The body diode of M1 pulls SOURCE to a diode above SENSE. Since M2 is off and its body diode is in the reverse blocking mode, the negative voltage is blocked by the V_{DS} of M2.

Figure 6 shows the waveforms when the application circuit in Figure 5 is hot plugged to –24V. Due to the parasitic inductance at IN, SENSE and GATE, the voltages ring significantly below –24V. The TransZorb helps to clamp the negative undershoot and a 40V MOSFET is selected for M2 to survive this undershoot.

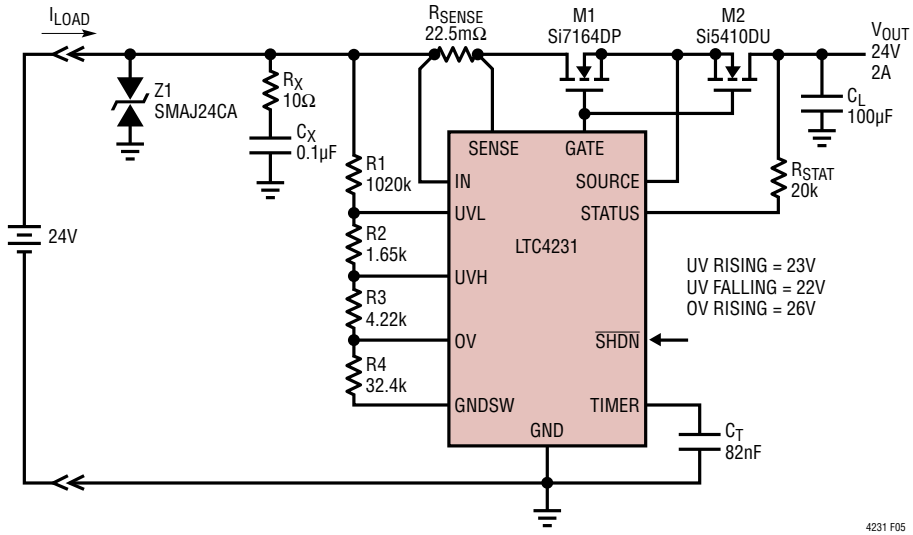


Figure 5. Back-to-Back MOSFETs Protect Against Reverse Input

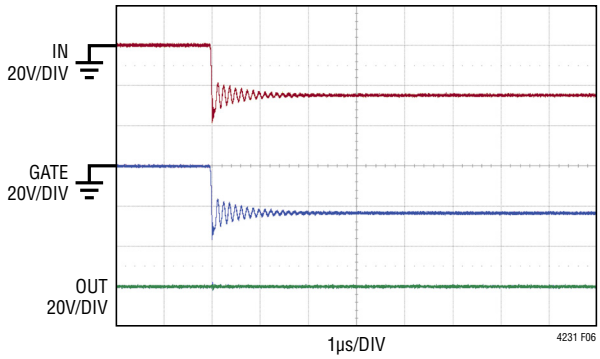


Figure 6. LTC4231 in Reverse Input Mode

APPLICATIONS INFORMATION

Achieving Low Quiescent Current

Table 1 summarizes the average I_{CC} of the various operating modes of the LTC4231.

Table 1.

MODE	I_{CC} (NORM)	I_{CC} (MAX)
Start-Up or Overcurrent	300µA	600µA
Debounce, Normal On, Voltage or Current Fault	4µA	10µA
Shutdown	0.3µA	1µA
Reverse Input	–2.5mA	–5mA

To lower I_{CC} when GATE is high, the LTC4231 operates in normal on mode, where the charge pump delivers pulses of current to the GATE capacitance (either an external C_G or the parasitic capacitance of the external MOSFETs) to boost ΔV_{GATE} to $\Delta V_{GATE(H)}$ followed by sleep periods when the GATE capacitance holds up GATE. Leakage will cause ΔV_{GATE} to droop during these sleep periods. When the ΔV_{GATE} low comparator detects ΔV_{GATE} drooping by more than 0.7V, it will activate the charge pump to boost ΔV_{GATE} back to $\Delta V_{GATE(H)}$ before returning to sleep mode. In addition to the ΔV_{GATE} low comparator, there is a charge pump refresh timer that turns on the charge pump every 15ms to boost ΔV_{GATE} back to $\Delta V_{GATE(H)}$. This timer is reset when the charge pump turns on.

When in charge pump sleep mode the LTC4231 consumes 2µA. When the charge pump is on to deliver a current pulse to GATE, I_{CC} briefly goes up to 200µA. The amount of leakage at GATE ($I_{GATE(LEAKAGE)}$) will determine the duty cycle of the charge pump. Figure 7 shows start-up and ΔV_{GATE} regulation (with different $I_{GATE(LEAKAGE)}$) waveforms from the Figure 5 application circuit.

As the average current delivered to GATE during the current pulse is around 15µA, the duty cycle of the charge pump for a $I_{GATE(LEAKAGE)}$ of 0.1µA is 0.1/15 = 0.67%. The average current due to ΔV_{GATE} regulation is then 0.67% • 200µA = 1.3µA. When added to the average current due to OV/UV strobing (0.7µA) and charge pump sleep mode current (2µA), the average quiescent current of the LTC4231 during the normal on mode is 1.3µA + 0.7µA + 2µA = 4µA. The normal on mode average supply current can be estimated using the formula:

$$I_{CC} = 2.7\mu A + 13.3 \bullet I_{GATE(LEAKAGE)}$$

The Typical Performance Characteristics section shows a graph of average I_{CC} (normal on) against $I_{GATE(LEAKAGE)}$.

Shutdown Mode

When $\overline{SHDN}$ goes low, STATUS pulls low and a 1mA pull-down will be activated between GATE and GND to cut off the external MOSFET. When GATE reaches <1.2V, I_{CC} drops to 0.3µA as the LTC4231 goes into shutdown mode. When $\overline{SHDN}$ goes high, GATE ramps up after the 40ms debounce cycle. Figure 8 shows the application in Figure 5 going into shutdown mode.

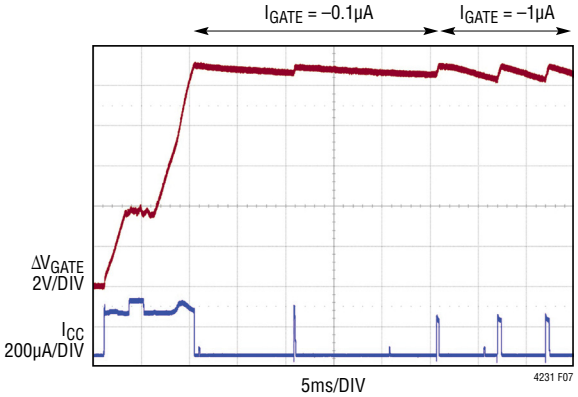


Figure 7. Regulating ΔV_{GATE} During Normal On Mode

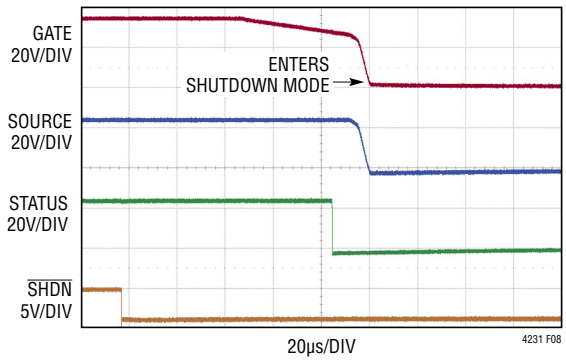


Figure 8. $\overline{SHDN}$ Going Low Activates Shutdown Mode

APPLICATIONS INFORMATION

Supply Transient Protection

When the capacitances at the input and output are very small, rapid changes in current during an output short-circuit event can cause transients that exceed the 40V absolute maximum ratings of IN, SENSE and SOURCE. To minimize such spikes, use wider traces or heavier trace plating to reduce the power trace inductance. Also, bypass locally with a 10µF electrolytic and 0.1µF ceramic if hot plug inrush current is not a concern. Alternatively, clamp the input with a transient voltage suppressor (Z1 in Figure 5). A 10Ω, 0.1µF snubber damps the response and reduces ringing (R_X and C_X inFigure 5).

Design Example

As a design example, take the following specifications for the Figure 5 application circuit. The application is rated for a V_{IN} of 24V at 2A, C_L = 100µF. UV rising = 23V, UV falling = 22V, OV rising = 26V.

Sense resistor:

$$R_{SENSE} = \frac{\Delta V_{SENSE(CB)(MIN)}}{2A} = \frac{47mV}{2A} = 23.5m\Omega$$

Use R_{SENSE} = 22.5mΩ for margin. Worst case analog current limit:

$$I_{LIMIT(MIN)} = \frac{\Delta V_{SENSE(ACL)(MIN)}}{22.5m\Omega} = \frac{65mV}{22.5m\Omega} = 2.89A$$

$$I_{LIMIT(MAX)} = \frac{\Delta V_{SENSE(ACL)(MAX)}}{22.5m\Omega} = \frac{90mV}{22.5m\Omega} = 4A$$

Calculate the worst case time it takes to charge up C_L in analog current limit:

$$t_{CHARGE(MAX)} = \frac{C_L \bullet V_{IN}}{I_{LIMIT(MIN)}} = \frac{100\mu F \bullet 24V}{2.89A} = 0.9ms$$

For inrush control using analog current limit, $t_{CHARGE(MAX)}$ must be less than the circuit breaker delay (t_{CB}) for a proper start-up.

The worst case power dissipation in MOSFET M1 occurs during a severe overcurrent fault when the current is controlled by analog current limit for the duration of t_{CB}:

$$P_{DISS} = V_{IN} \bullet I_{LIMIT(MAX)} = 24V \bullet 4A = 96W$$

The SOA (safe operating area) curve for the Si7164DP MOSFET shows that it can withstand 180W for 10ms. So choose a t_{CB} that is less than 10ms but higher than 0.9ms ($t_{CHARGE(MAX)}$). In this case, use t_{CB} = 2ms.

$$C_T = \frac{t_{CB}}{24} = \frac{2ms}{24} = 0.082\mu F = 82nF$$

If a low inrush current (< $\Delta V_{SENSE(CB)}$) is preferred, refer to the Figure 1 application circuit which uses a gate capacitor C_G to limit the inrush current. Choose I_{INRUSH} = 0.5A which is set using C_G:

$$C_G = \frac{C_L}{I_{INRUSH}} \bullet 10\mu A = \frac{1000\mu F}{0.5A} \bullet 10\mu A = 20nF$$

The time to charge up C_L with 0.5A is:

$$t_{CHARGE} = \frac{C_L \bullet V_{IN}}{I_{INRUSH}} = \frac{1000\mu F \bullet 24V}{0.5A} = 48ms$$

In this case t_{CHARGE} can be longer than t_{CB} with no start-up issue.

The average power dissipation in the MOSFET M1 during this start-up is:

$$P_{DISS} = \frac{V_{IN} \bullet I_{INRUSH}}{2} = \frac{24V \bullet 0.5A}{2} = 6W$$

The SOA of the MOSFET M1 must be evaluated to ensure that it can withstand 6W for 48ms. The SOA curve of the Si7120ADN withstands 10W for 360ms, satisfying the requirement.

The purpose of MOSFET M2 is to block the reverse path from OUT (drain of M2) to IN when GATE pulls to GND so that IN can go lower than OUT or even negative. Choose a 40V MOSFET to withstand a worse case reverse DC voltage of –24V. The Si5410DU offers a good choice with a maximum $R_{DS(ON)}$ of 18mΩ at V_{GS} = 10V.

APPLICATIONS INFORMATION

The IN monitoring resistors R1–R4 should be chosen to yield a total divider resistance of between 1M to 2M for both low power and good transient response. Using the formulas from the Monitor OV and UV Faults section, R1–R4 are calculated as follows (with all resistor values rounded up to the nearest 1% accurate standard values):

Choose R1 + R2 + R3 + R4 = 1000kΩ

$$R4 = \left(\frac{0.795V}{V_{OVOFF}}\right) \bullet 1000k\Omega$$

Choose R4 = 32.4kΩ to give total divider resistance: R1 + R2 + R3 + R4 = 1060kΩ.

$$R3 = \left(\frac{V_{OVOFF}}{V_{UVON}} - 1\right) \bullet R4 = \left(\frac{26V}{23V} - 1\right) \bullet 32.4k\Omega = 4.22k\Omega$$

$$R2 = \left(\frac{V_{UVON}}{V_{UVOFF}} - 1\right) \bullet \left(\frac{V_{OVOFF}}{V_{UVON}}\right) \bullet R4$$

$$= \left(\frac{23V}{22V} - 1\right) \bullet \left(\frac{26V}{23V}\right) \bullet 32.4k\Omega = 1.65k\Omega$$

$$R1 = \left(\frac{V_{OVOFF}}{0.795V} - 1\right) \bullet R4 - R3 - R2$$

Layout Considerations

To achieve accurate current sensing, a Kelvin connection for the sense resistor is recommended. The PCB layout for the resistor should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation. In Hot Swap applications where load currents can be high, narrow PCB tracks exhibit more resistance than wider tracks and operate at elevated temperatures. 1oz copper exhibits a sheet resistance of about 0.5mΩ/square. The minimum trace width for 1oz copper foil is 0.5mm per amp to make sure the trace stays at a reasonable temperature. Using 0.8mm per amp or wider is recommended. Thicker top and bottom copper such as 3oz or more can improve electrical conduction and reduce PCB trace dissipation.

If a resistor R5 (see Figure 1) is used, place it as close as possible to M1's gate input. This will limit the parasitic trace capacitance that leads to M1 self-oscillation. The transient voltage suppressor, Z1, when used, should be mounted close to the LTC4231 using short lead lengths. A recommended PCB layout for the sense resistor and back-to back power MOSFETs is shown in Figure 9.

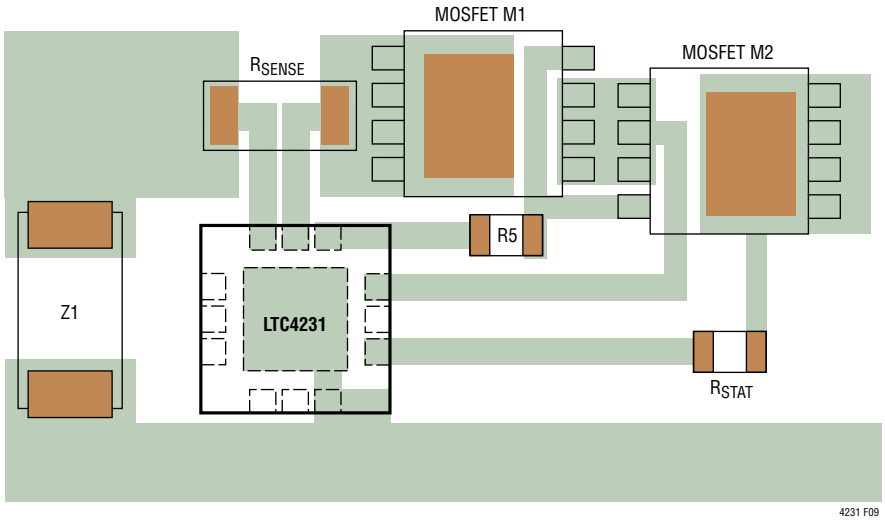


Figure 9. Recommended Layout

APPLICATIONS INFORMATION

Additional Applications

Figure 10 shows a reverse-battery protected application featuring the LTC2955 micropower push-button controller. A press on the push button switch will turn on the LTC4231 while a subsequent press will turn off the LTC4231. In the event the LTC4231 is unable to power-up successfully when EN goes high, the STATUS output is fed back to the $\overline{KILL}$ input in order to place the LTC4231 back in the very low-power Shutdown mode.

Figure 11 illustrates a 36V application with an UV rising threshold of 35V, an UV falling threshold of 33V and an OV rising threshold of 38V. As the IN operating voltage is so near to its 40V absolute maximum rating, a suitable TransZorb is not available to protect IN. Instead, a floating GND architecture is used to help the LTC4231 survive possible voltage transients during short circuit events. This architecture is strictly for handling IN transients during 36V operation. It does not allow DC V_{IN} operation > 39V.

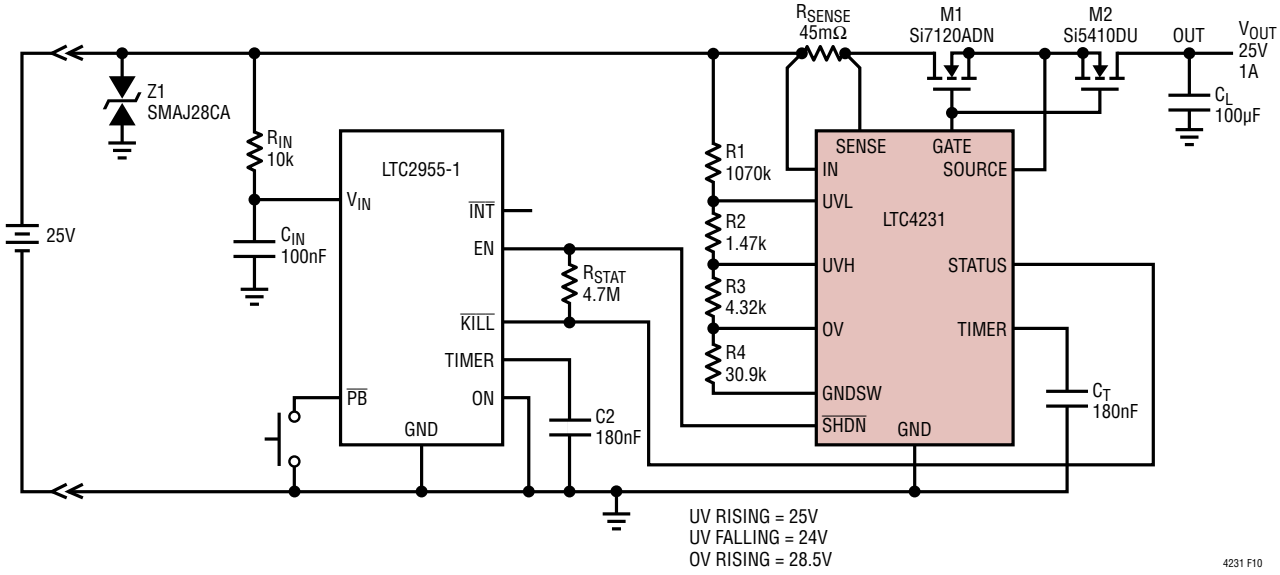
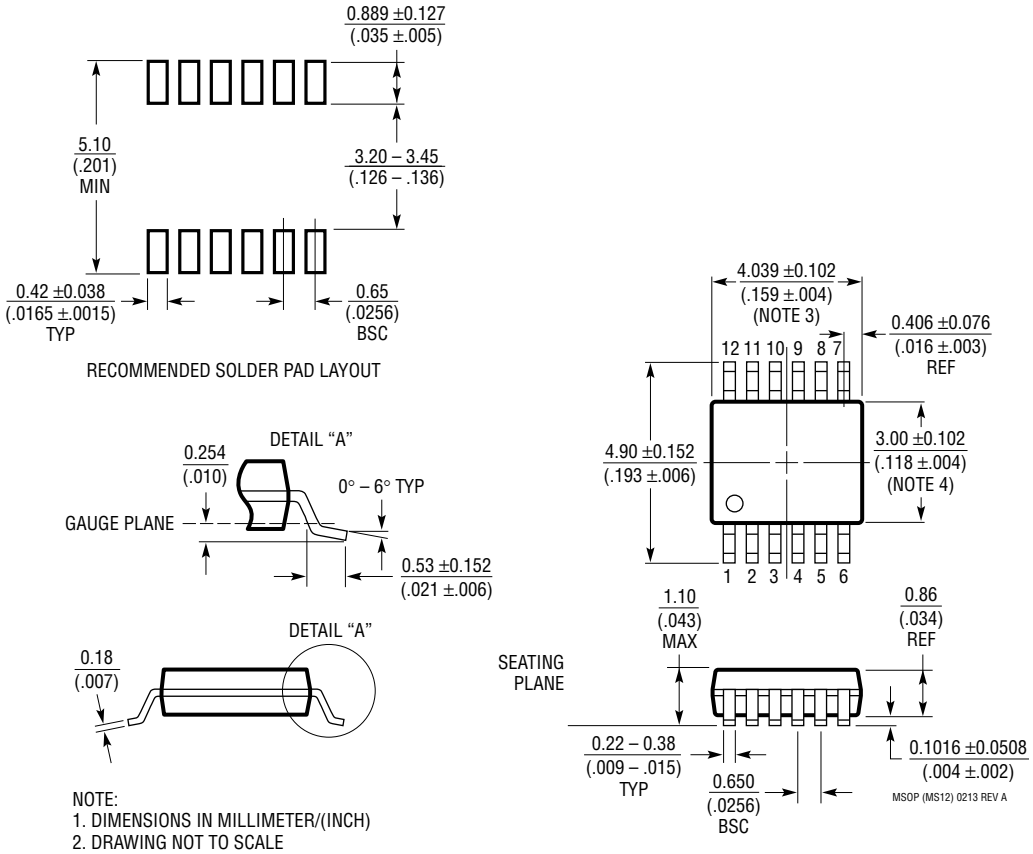


Figure 10. Micropower Push Button and Hot Swap Controllers with Reverse Battery Protection

PACKAGE DESCRIPTION

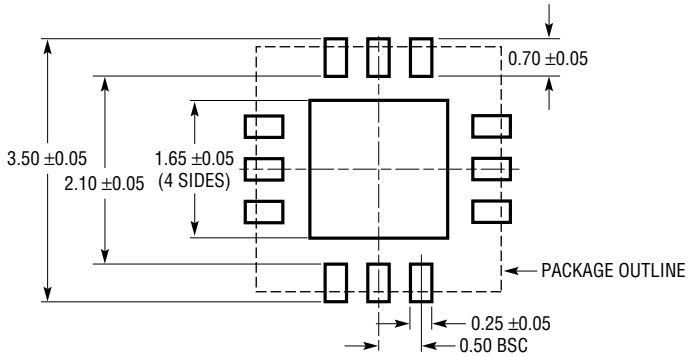
MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev A)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

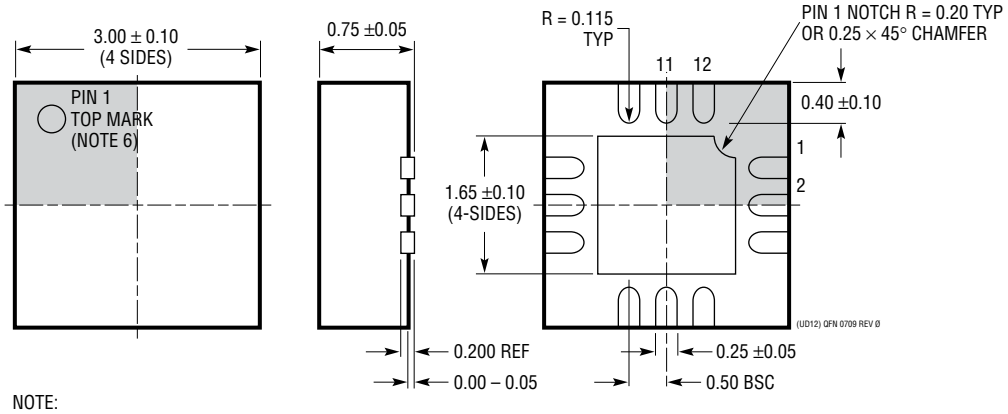
PACKAGE DESCRIPTION

UD Package
12-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1855 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/15	Added H-grade information	2, 3, 4
		Updated specifications: $V_{GATE(L)}$, $I_{GATE(UP)}$, $t_{D(ON)}$, t_{RETRY}, t_{PERIOD}, t_{SAMPLE}, t_{CB}	3,4
B	08/19	Added AEC-Q100	1, 3

TYPICAL APPLICATION

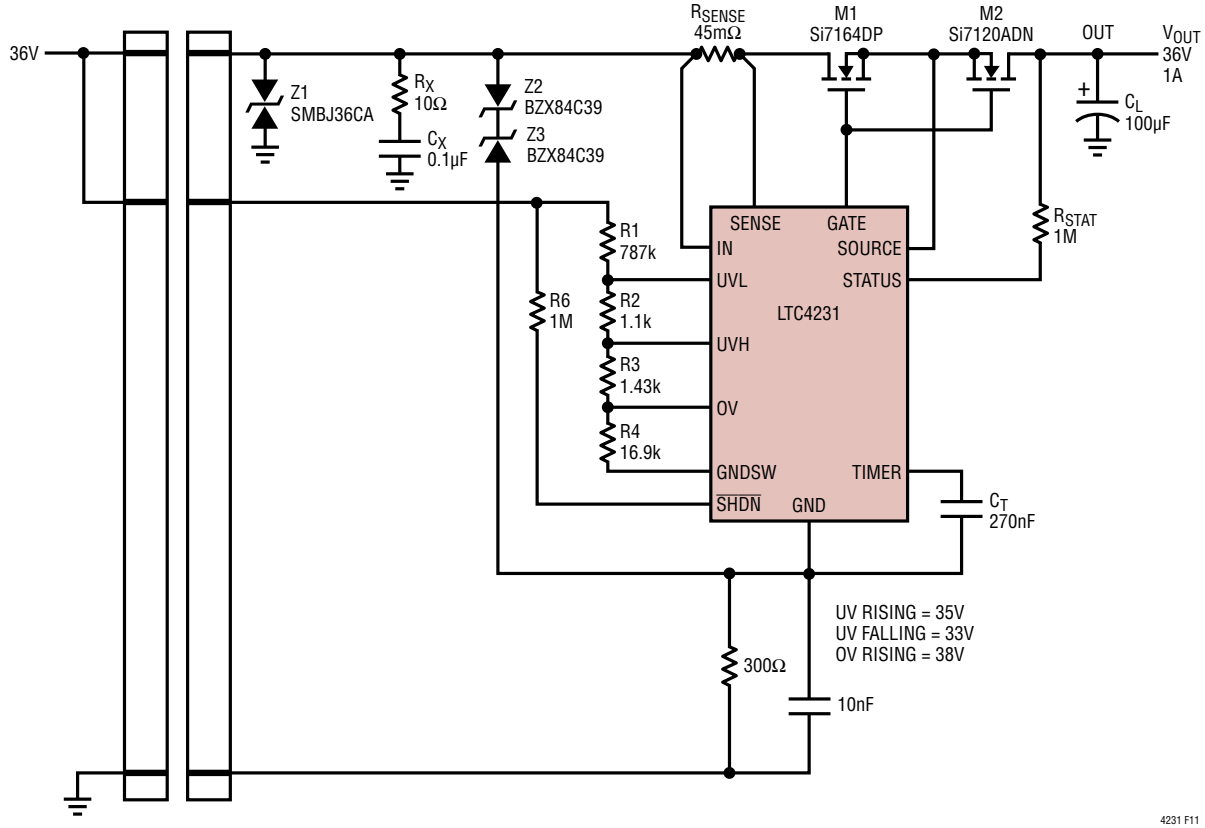


Figure 11. 36V Hot Swap Application with Reverse Protection

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4361	Overvoltage/Overcurrent Protection Controller	220µA I_Q, 2.5V to 5.5V Operation, 80V Protection
LTC4365	OV, UV and Reverse Supply Protection Controller	25µA I_Q, 2.5V to 34V Operation, –40V Reverse Input
LTC4359	Ideal Diode Controller with Reverse Input Protection	150µA I_Q, 9µA in Shutdown, 4V to 80V Operation
LTC4364	Surge Stopper/Hot Swap with Ideal Diode	370µA I_{CC}, 4V to 80V Operation, –40V Reverse Input, –20V Reverse Output
LTC2960	Nano-Current Dual Voltage Monitor	850nA I_Q, 2.5V to 36V Operation, 1.5% Accuracy
LTC4229	Ideal Diode and Hot Swap Controller	2.9V to 18V Operation, 2mA I_{IN}, 0.5µs Ideal Diode Turn-On/Off
LTC4232	5A Integrated Hot Swap Controller	Integrated 33mΩ MOSFET with Sense Resistor, 2.9V to 15V Operation
LTC2955	Pushbutton On/Off Controller	Automatic Turn-On, 1.2µA I_Q, 1.5V to 36V Operation
LTC4417	Prioritized PowerPath™ Controller	28µA I_Q, 2.5V to 36V Operation, –42V Reverse Input

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

LTC4231HMS-1#PBF LTC4231CUD-2#TRPBF LTC4231HMS-2#TRPBF LTC4231HMS-1#TRPBF LTC4231CMS-1#TRPBF LTC4231HUD-1#PBF LTC4231IMS-2#TRPBF LTC4231CUD-1#PBF LTC4231HUD-2#TRPBF LTC4231IUD-2#PBF LTC4231CUD-2#PBF LTC4231IUD-1#PBF LTC4231IUD-2#TRPBF LTC4231HMS-2#PBF LTC4231HUD-2#PBF LTC4231IMS-1#TRPBF LTC4231CMS-2#TRPBF LTC4231IMS-2#PBF LTC4231CMS-2#PBF LTC4231HUD-1#TRPBF LTC4231CMS-1#PBF LTC4231IUD-1#TRPBF LTC4231IMS-1#PBF LTC4231CUD-1#TRPBF DC2161A-A DC2161A-B LTC4231HMS-1#WPBF LTC4231HMS-1#WTRPBF LTC4231HMS-2#WPBF LTC4231HMS-2#WTRPBF